WHAT IS CLAIMED IS:

1. A chip-stack semiconductor device, comprising multiple semiconductor chips vertically stacked on top of each other,

wherein:

each of the semiconductor chips includes multiple through electrodes connected to each other in regions inside of electrode pads derived from a device region, each of the through electrodes linking a front surface to a back surface of the semiconductor chip.

2. The chip-stack semiconductor device as set forth in claim 1, wherein the electrode pads are provided along a periphery of the semiconductor chip so as to surround the device region.

3. The chip-stack semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to the electrode pad.

4. The chip-stack semiconductor device as set forth in claim 2, wherein at least one type of the through electrodes is contact through electrodes electrically connected to the

electrode pad.

5. The chip-stack semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is non-contact through electrodes not electrically connected to the electrode pad.

6. The chip-stack semiconductor device as set forth in claim 2, wherein at least one type of the through electrodes is non-contact through electrodes not electrically connected to the electrode pad.

7. The chip-stack semiconductor device as set forth in claim 1, wherein a through electrode is further provided in regions outside of the electrode pad.

8. The chip-stack semiconductor device as set forth in claim 2, wherein a through electrode is further provided in regions outside of the electrode pad.

9. The chip-stack semiconductor device as set forth in claim 1, wherein the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other.

10. The chip-stack semiconductor device as set forth in claim 2, wherein the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other.

11. A manufacturing method of a chip-stack semiconductor device, comprising:

semiconductor chip manufacturing step of forming semiconductor chips; and

semiconductor chip stacking step of stacking a plurality of the multiple semiconductor chip,

the semiconductor chip manufacturing step including the steps of:

(a) using a mask having an opening with a predetermined shape in a region inside of an electrode pad derived from a device region, forming a groove being made through the electrode pad and having a predetermined depth in the semiconductor chip;

(b) forming an insulating film on an inside wall of the groove;

(c) filling the groove with a conductive material; and

(d) forming the through electrode made of the conductive material linking a front surface to a back

surface of the semiconductor chip by removing a back surface of the semiconductor chip partially in a thickness direction to expose the conductive material,

the steps (a)-(d) being carried out in this order.

12. The manufacturing method as set forth in claim 11, wherein the semiconductor chip manufacturing step includes step of removing the insulating film formed on the inside wall of the groove in the same layer as the electrode pad between the steps (b) and (c).

13. The manufacturing method as set forth in claim 11, wherein the semiconductor chip manufacturing step includes step of further forming a through electrode in regions outside of the electrode pad.

14. The manufacturing method as set forth in claim 12, wherein the semiconductor chip manufacturing step includes step of further forming a through electrode in regions outside of the electrode pad.

15. The manufacturing method as set forth in claim 11, wherein the semiconductor chip manufacturing step includes step of forming the electrode pad derived from the device region before the step (a),

in the step of forming the electrode pad, the electrode pad is formed with its space saved by changing the mask, and

the semiconductor chip manufacturing step further includes step of forming a through electrode in a region made available by the formation of the electrode pad with its space saved.

16. The manufacturing method as set forth in claim 12, wherein the semiconductor chip manufacturing step includes step of forming the electrode pad derived from the device region before the step (a),

in the step of forming the electrode pad, the electrode pad is formed with its space saved by changing the mask, and

the semiconductor chip manufacturing step further includes step of forming a through electrode in a region made available by the formation of the electrode pad with its space saved.

17. The manufacturing method as set forth in claim 11, wherein in the step (a) of the semiconductor chip manufacturing step, a plurality of the groove is formed in a region inside of the electrode pad.

18. The manufacturing method as set forth in claim 12, wherein in the step (a) of the semiconductor chip manufacturing step, a plurality of the groove is formed in a region inside of the electrode pad.